UniSA | Institute for Telecommunications Research

Software Defined Radio Research at ITR

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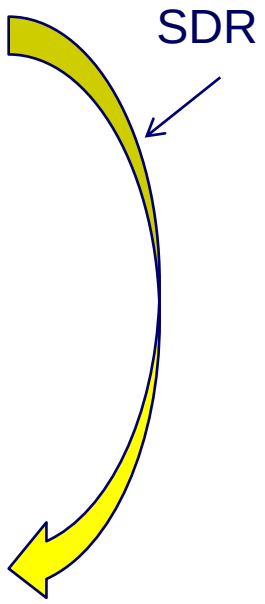
Outline

- Introduction for ITR
  - Advanced Prototyping Lab facilities
- SDR Research Topics
  - SDR Facilities
  - Implementation Methodology
  - Software Communications Architecture
  - Runtime Reconfiguration
- SDR Projects
  - SANLab
  - Australia Space Research Program
  - Other Projects

Institute for Telecommunications Research

- The ITR has approximately 35 staff and 30 postgraduate students
- Research
  - Information Theory
  - PHY layer advanced algorithms
  - Computational and Theoretical Neuroscience
  - Free-space optical
- Engineering
  - Satellite Modems
  - Customized Wireless Transceiver system
  - Free-space optical Transceiver



Advanced Prototyping Lab

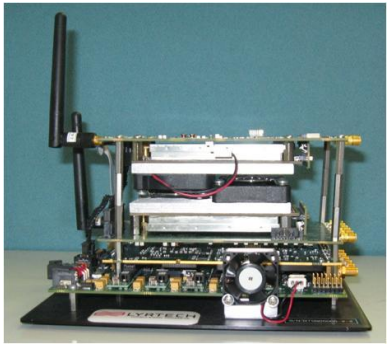
- Comprehensive design capabilities from prove concept Matlab simulation to real implementation
- GPP based: cluster and embedded system
- Signal Processing: FPGA and DSP
- Testing equipments:
  - High speed: 3.5 GHz oscilloscope and Ka Band spectrum analyser
  - broad range of general test equipment including signal generators, signal vector analysers, logic analysers and noise sources and bit error rate analysers

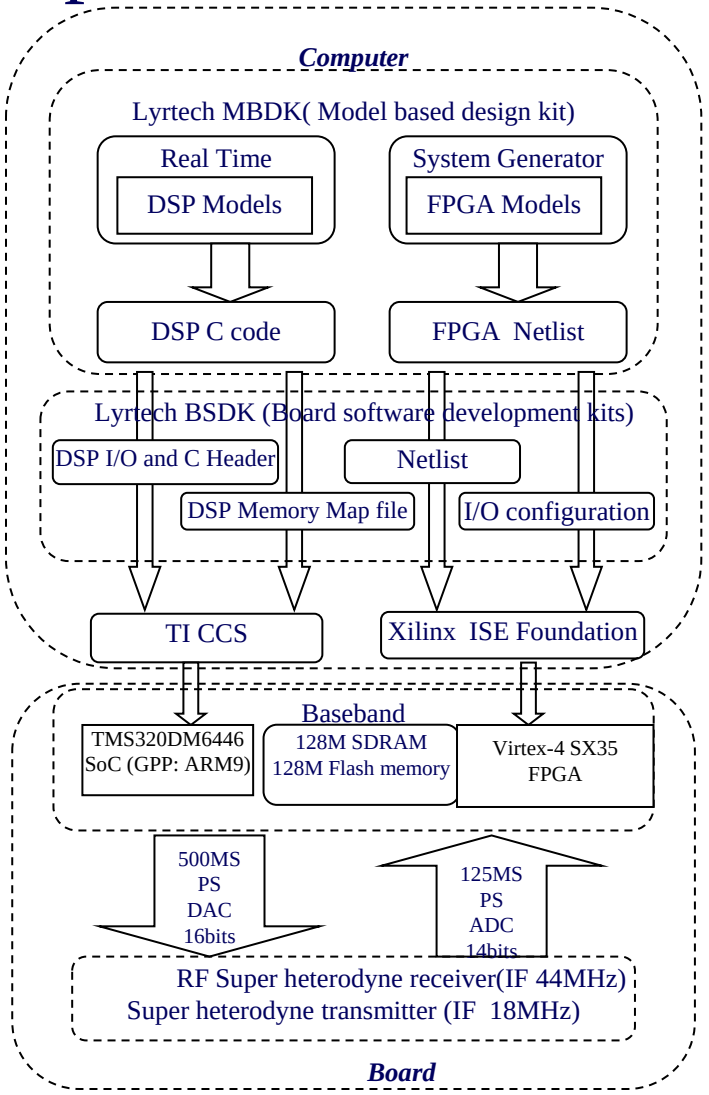
SDR Research at ITR

- SDR Facilities
  - Lyrtech
  - USRP
  - SDR4000
- Research Topic
  - Implementation Methodology
  - Software Communications Architecture
  - Runtime Reconfiguration

SDR Facilities : Lyrtech

- Small Form Factor (SFF) SDR platform
  - TI DaVinci SoC DM6446
  - Xilinx Virtex 4
  - 2 by 2 MIMO (20MHz)
  - 125Msps ADC 500Msps DAC
  - Fully integrated MBDK
  - Partial SCA support





SDR Facilities : USRP

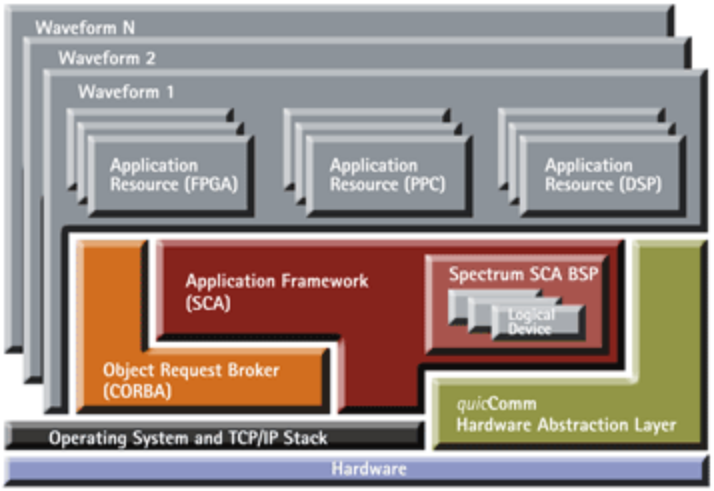
- CPU Based E210
- GPP Based E100
- GNU Radio
- OSSIE SCA Suite

- Main data processing are done in GPP/CPU, Coding in C/C++
  - difficult to guarantee real time signal processing
- FPGA can be coded in Simulink System-Generator
  - Very limited FPGA resource (Spartan 3)

SDR Facilities : Spectrum and CRC

- SDR4000
  - GPP: Power PC e500
  - DSP: TMS320C6416
  - FPGA: Xilinx Virtex-4 XC4VLX60

- quicComm
  - Driver/library
  - Communications
- SCA SCARI software suit
  - SCA Design Suite
  - Graphical interface

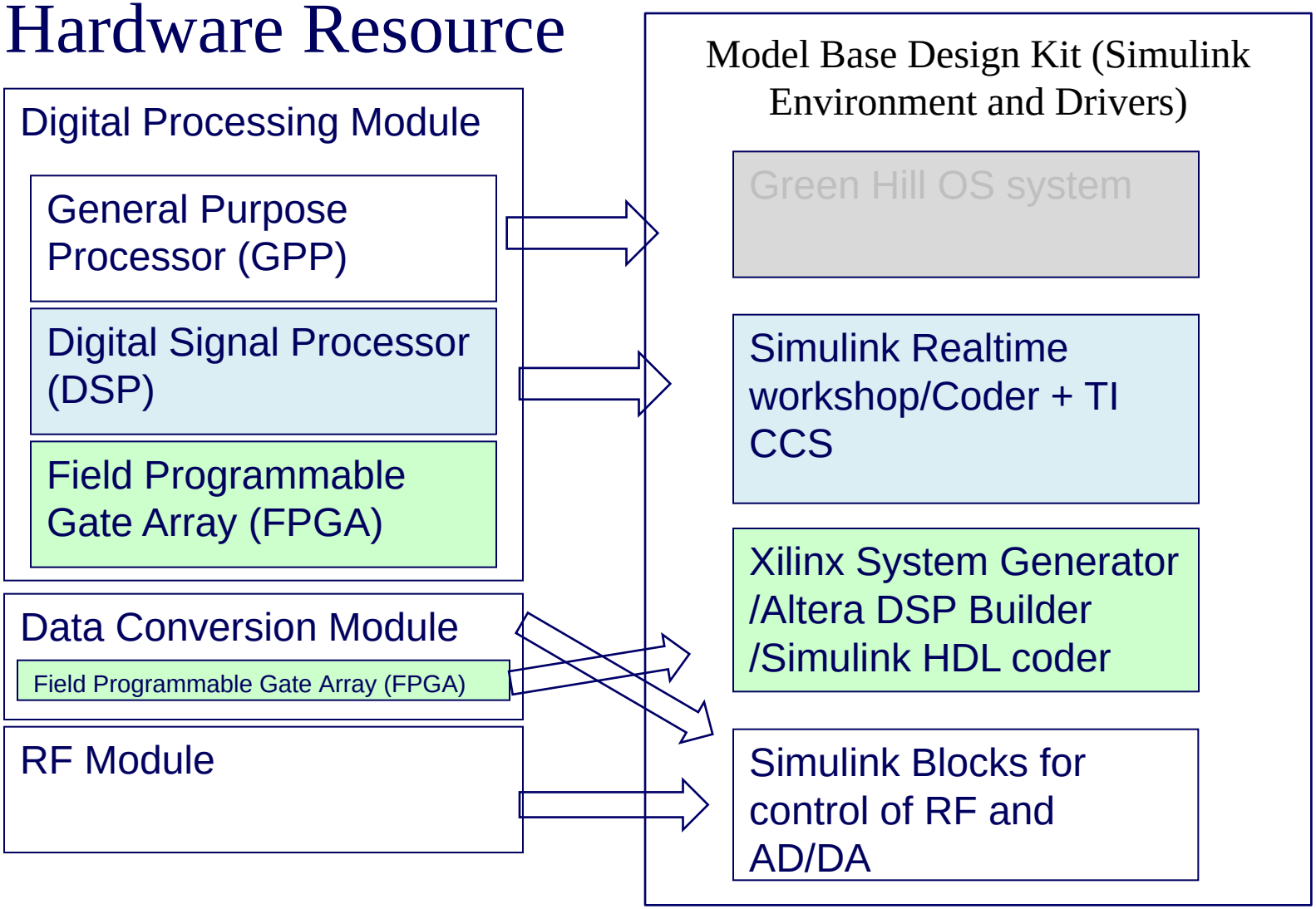


Implementation Methodology

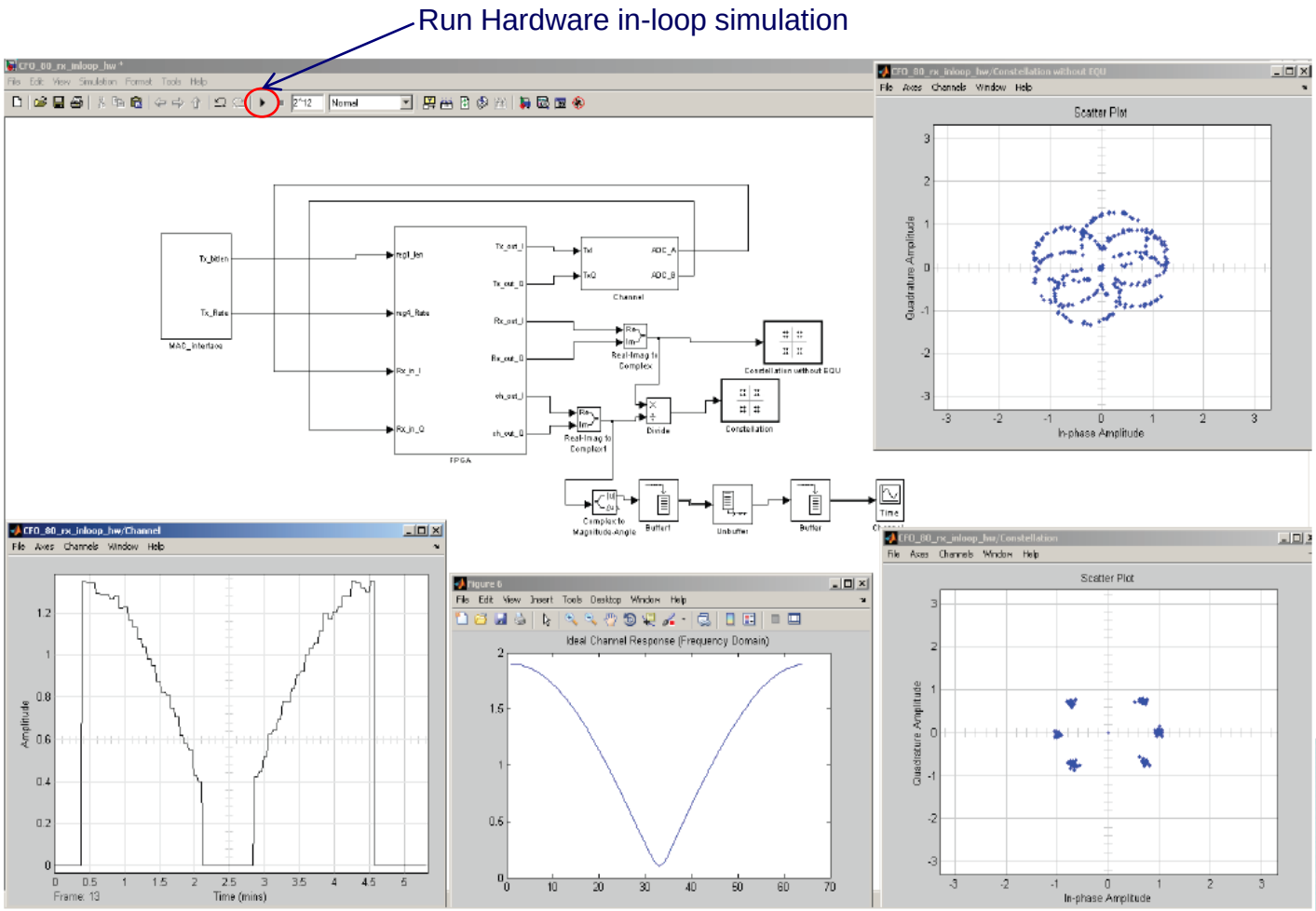
- Model Based Design (Simulink Environment)
  - Device Targeting
    - FPGA: System-Generator, HDL coder, DSP Builder
    - DSP: Real-time workshop, Matlab coder
  - System Level
    - RF and Analogue Control; HW image driver and downloads (Lyrtech)
- Benefits
  - Bridging the knowledge transaction gap
  - Fast Prototyping
  - Test environment
  - Graphical interface

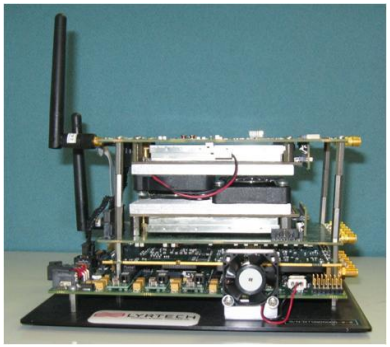
Implementation Methodology

- Hardware Resource



Implementation Methodology





Software Communications Architecture

- SCA
  - An open architecture framework that tells designers how elements of hardware and software are to operate in harmony within a software defined radio.
  - Enable cross platform waveform transfer.
  - SCA on GPP is available both as commercial or Open Source

ITR's research interests on SCA

- Evaluate existing SCA design tools
  - Cost of Resource when introducing SCA
  - Limitation and efficiency of SCA
  - How easy will it be to port SCA complied design between systems
- SCA for DSP and FPGA
  - Extend SCA to FPGA and DSP
    - Cost of HW resources
    - Impact on achievable speed
  - Run-time Reconfiguration?

Run-time reconfiguration

- Online reconfiguration
  - Crucial for Space SDR or low accessibility SDR applications
  - Important for systems with massive number of users
- FedSat (Australian built research satellite)
  - launched in 2002
  - an early adopter of reconfigurable technology for space-based communications
    - reconfigurable architecture for the payload & terminal
    - included a code uploader to reprogram the FPGA in orbit.

Run-time reconfiguration

- Main Challenge
  - System design level:
    - Memory
    - design of control signals
    - Backup channel
  - Communications:
    - Size of Hardware images could be big
    - Communication capabilities
    - Partial updates

Summary on SDR Research

- Implementation methodology is important
  - SDR: a combination of HW and SW
  - Development environment
    - Enable Hardware-in-loop simulation
  - No automatic code generation tool Matlab→FPGA
- SCA tools
  - SCA software doesn't support DSP and FPGA
  - No SCA integration with Matlab
- Partial reconfiguration
  - Plan during design stage.

SDR Project (application of SDR)

- SANLab WLAN PHY
- SDR in Space
- Other Projects

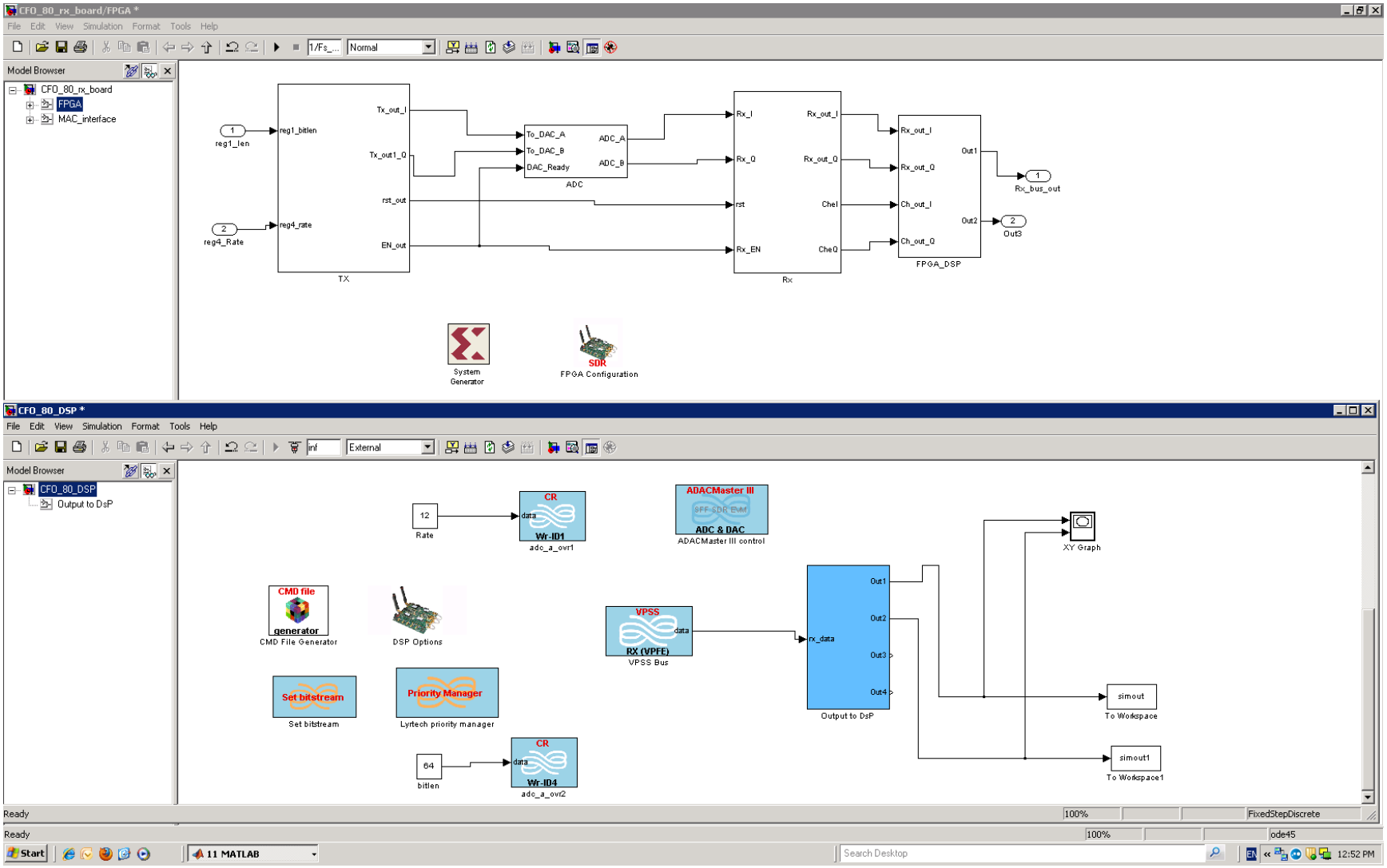
SDR Projects: SANLab

- South Australian Networking Laboratory (SANLab)
  - building a software defined radio (SDR) facility for physical layer and cross-layer experimentation and research.
  - An implementation for PHY of the WLAN 802.11g has been built/tested/compiled in Mathwork® Simulink & Real Time workshop& Xilinx ® system generator environment and run on the hardware through the model based design software.
  - Lyrtech platform

SANLab: WLAN PHY

- Full transmitter
- Receiver: Power Detection, CFO est., Sync, Channel est., Equalization, Phase Tracking, Deinterleaver, demapper, (Xilinx Decoder Core)
- Several testing models
- A brief time line regarding development is
  - Preparation and Hardware comparison: 1 FTE (Full-time equivalent)-month;
  - Software Study and Design: 6 FTE-month;
  - Hardware Testing and discussion: 3 FTE-month.

SANLab: FPGA and DSP in Simulink



SDR Projects: SDR in Space

- Supported by the Australian Space Research Program
- Satellite-enabled national wireless sensor network
- Developing and demonstrating software-defined radio technology for
  - space segment
  - ground station
  - terminals

SDR projects: Others

- Implementation of part of a high speed baseband wireless communication system
  - Clock speed over 250MHz
  - Data rate over 3Gbps
  - Model based design
- Consultant work about Lyrtech
- Student Projects
  - Radar signal processing
  - FPGA for computation in artificial Neural Network

Thanks

- Any Questions?